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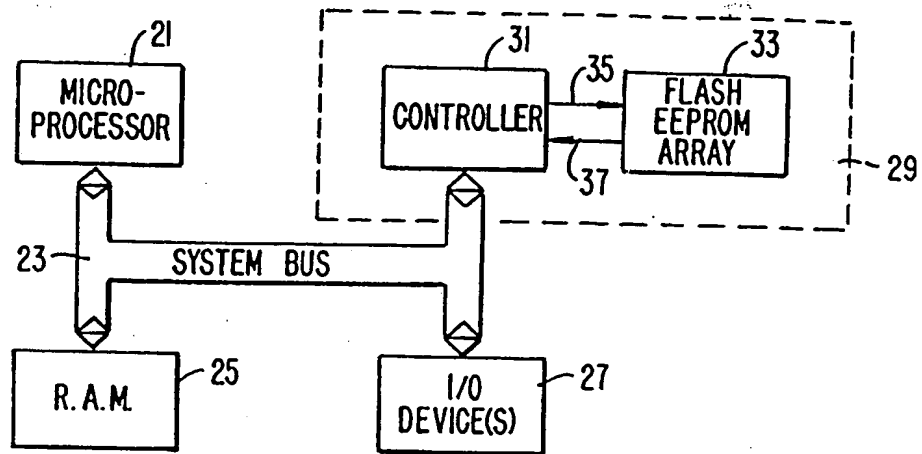


FIG. 1A

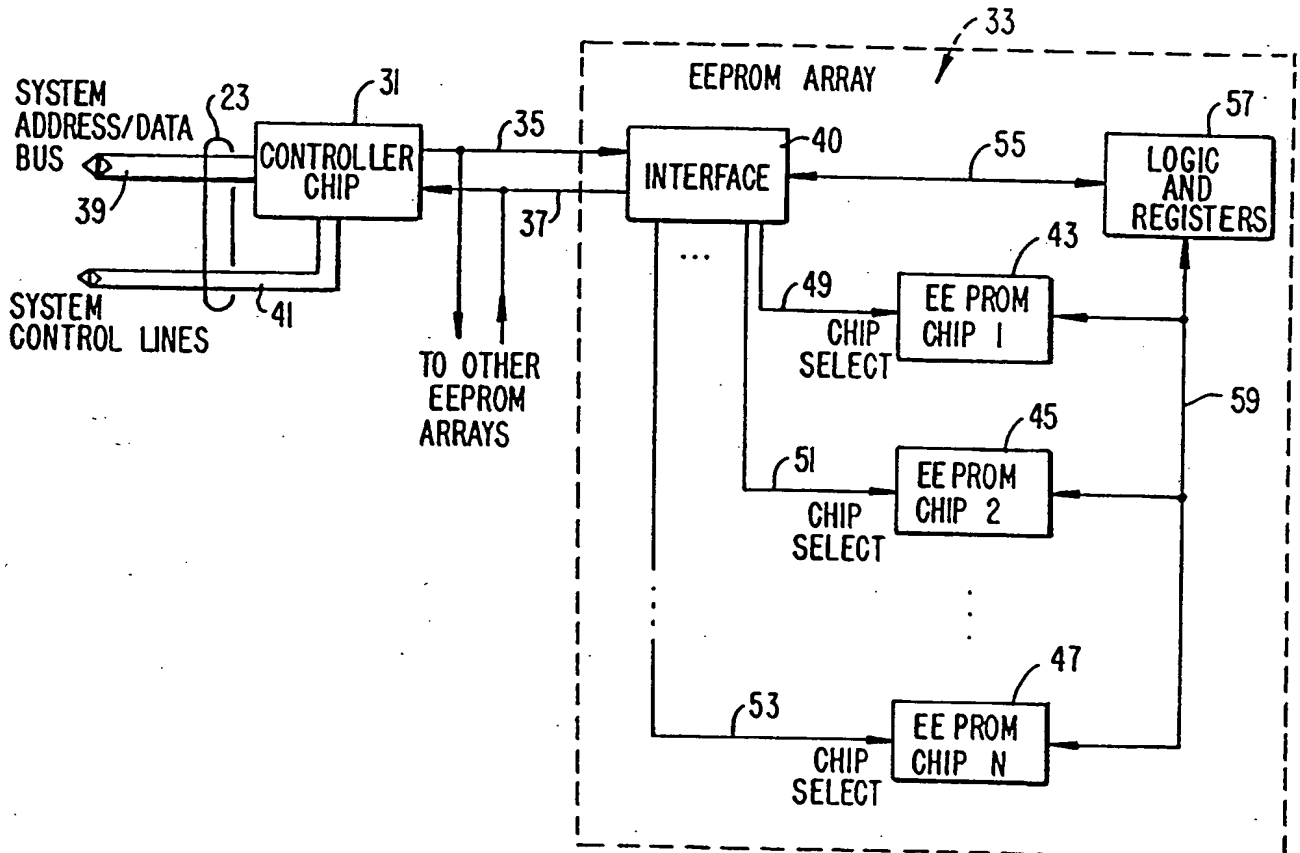


FIG. 1B

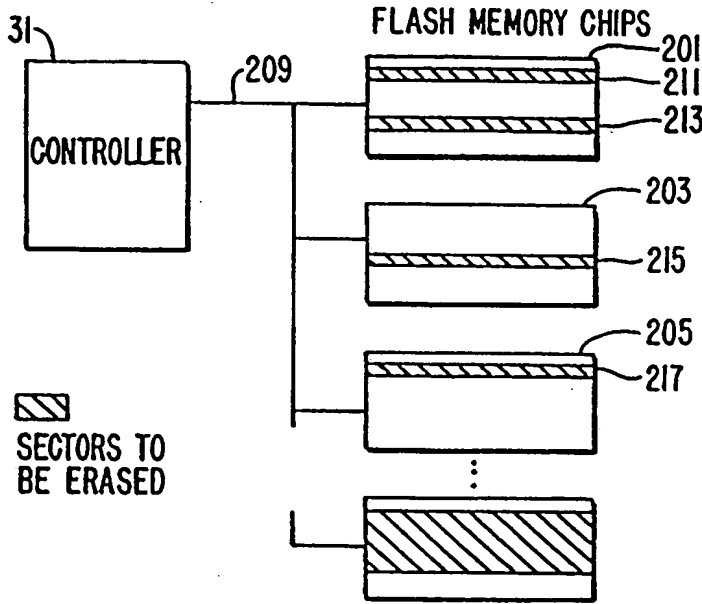


FIG. 2

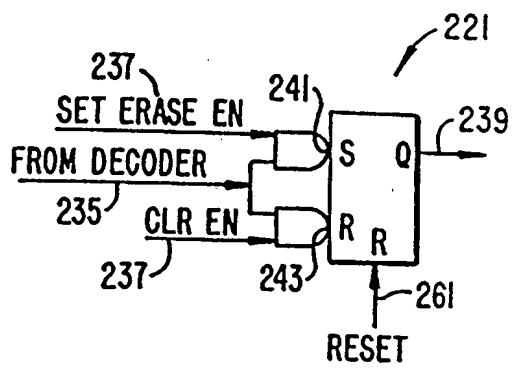


FIG. 3B

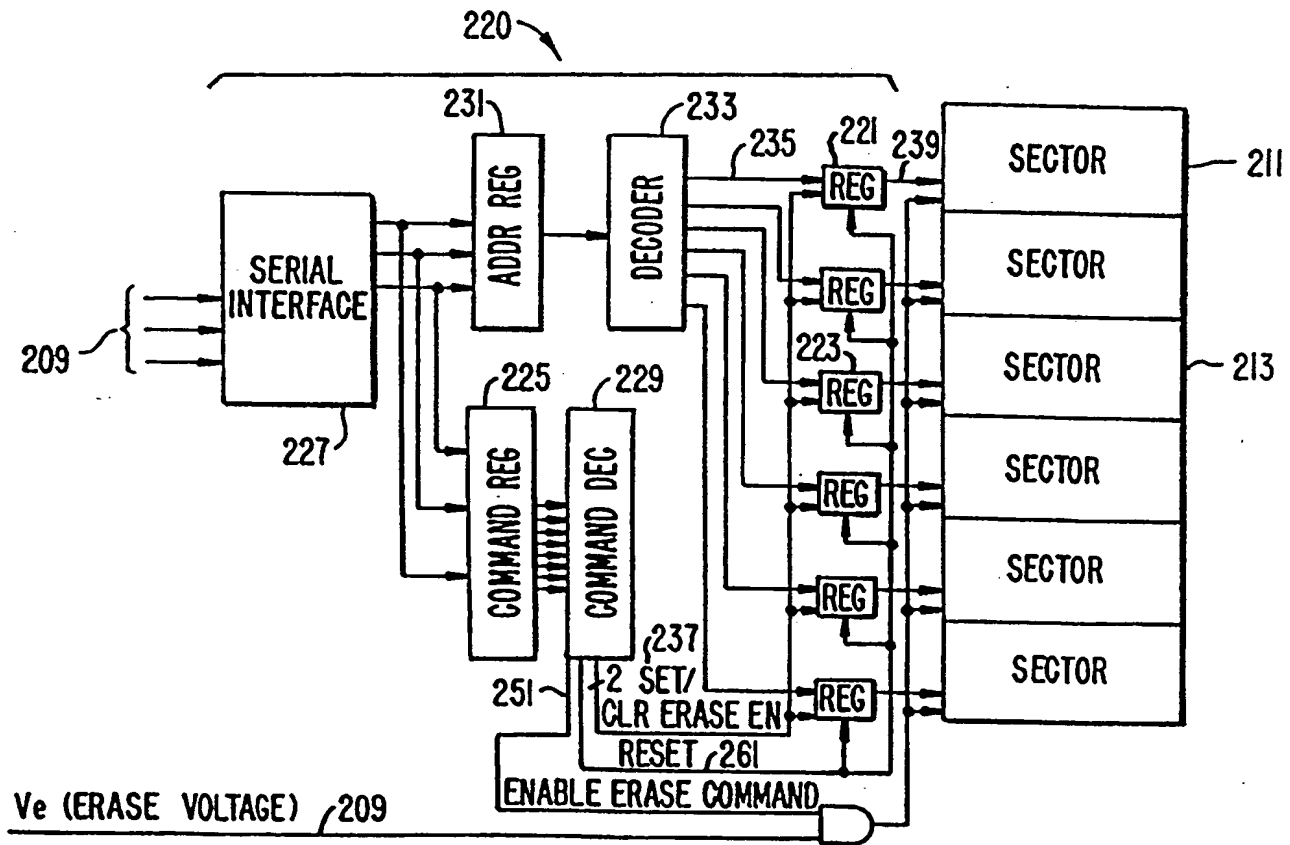


FIG. 3A



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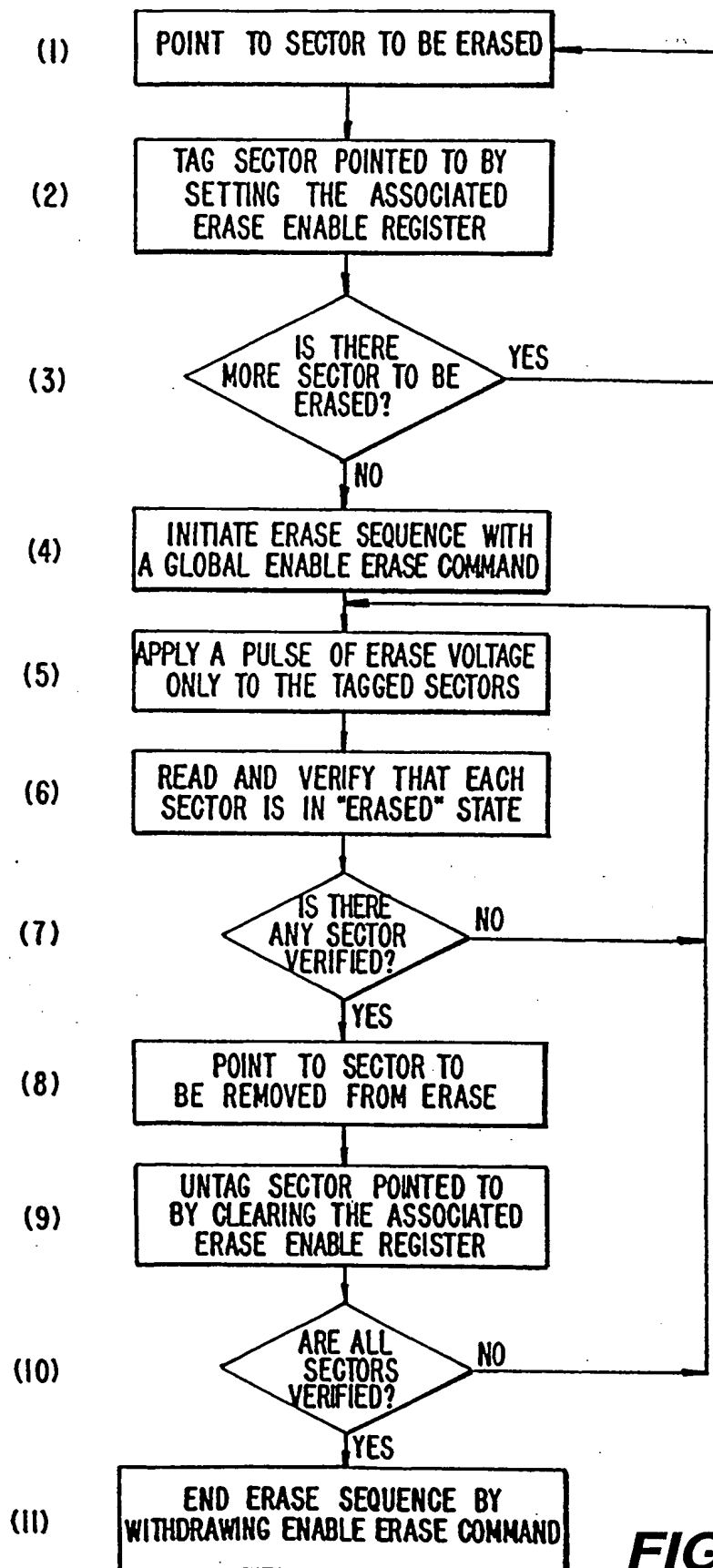


FIG._4

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FIG. 5

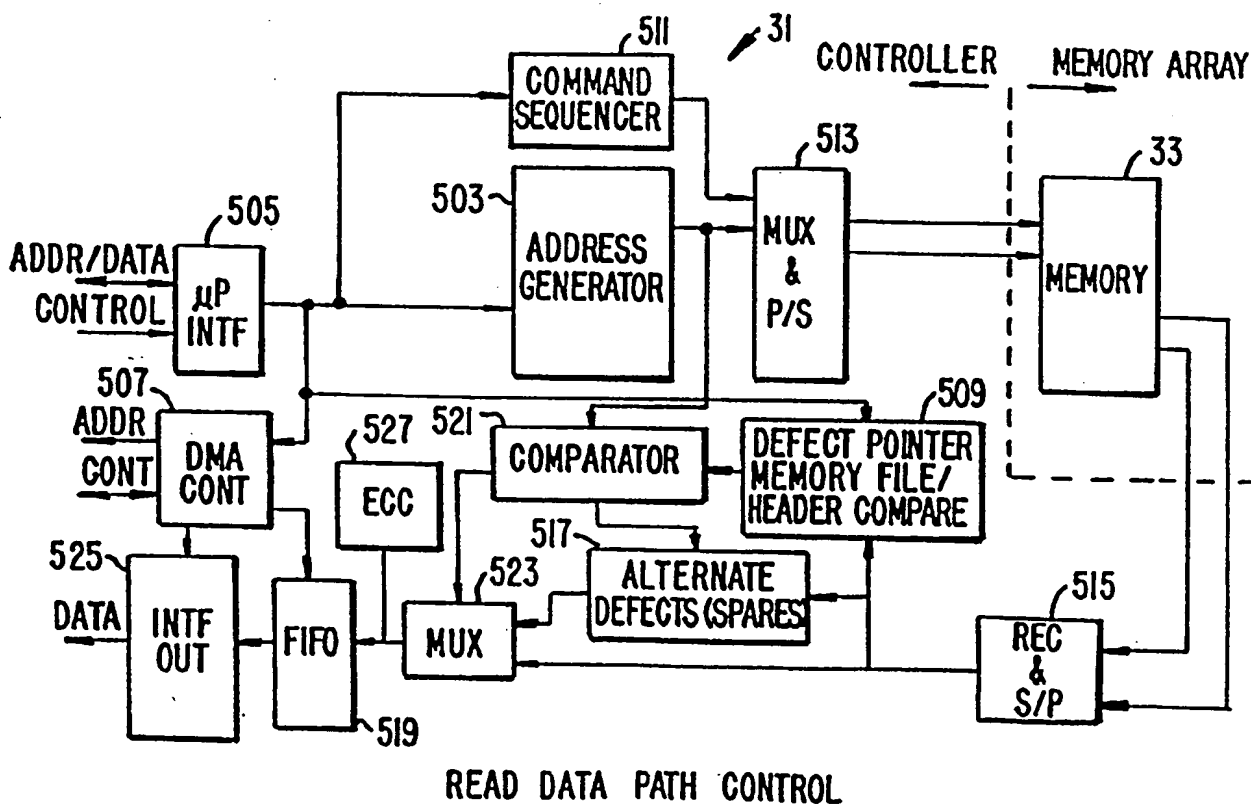
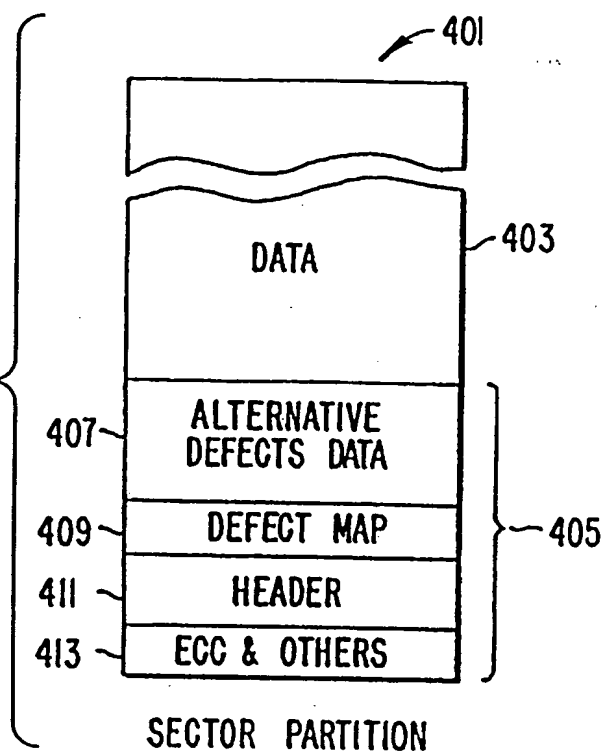


FIG. 6

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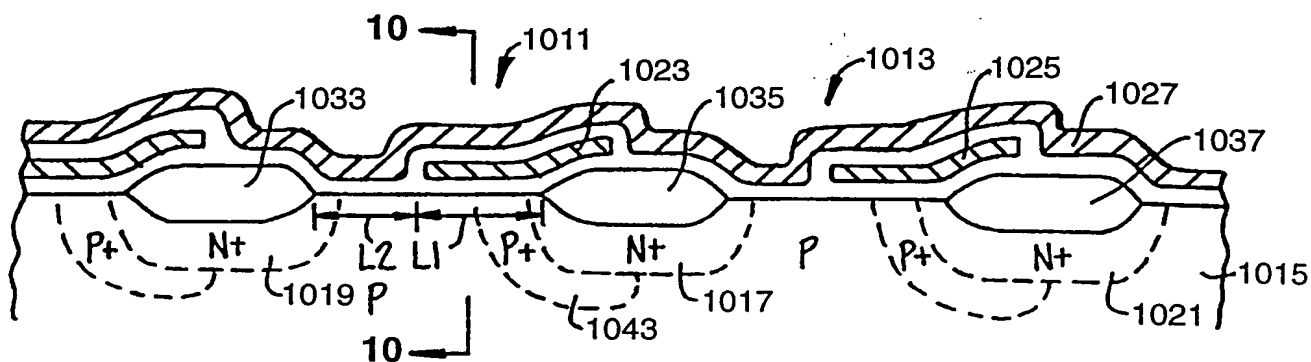


FIG. 9

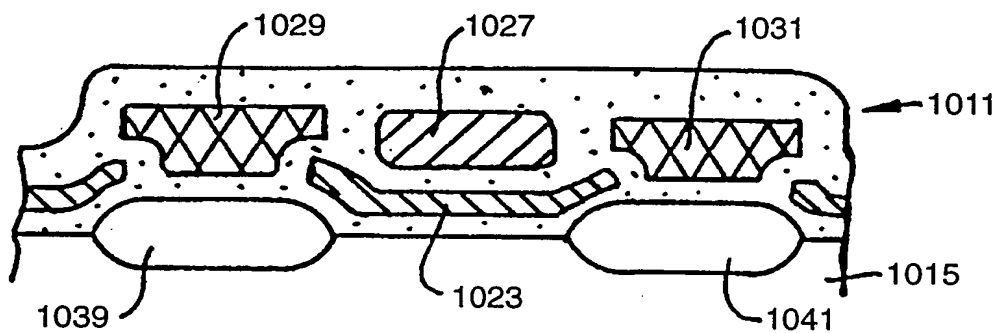


FIG. 10

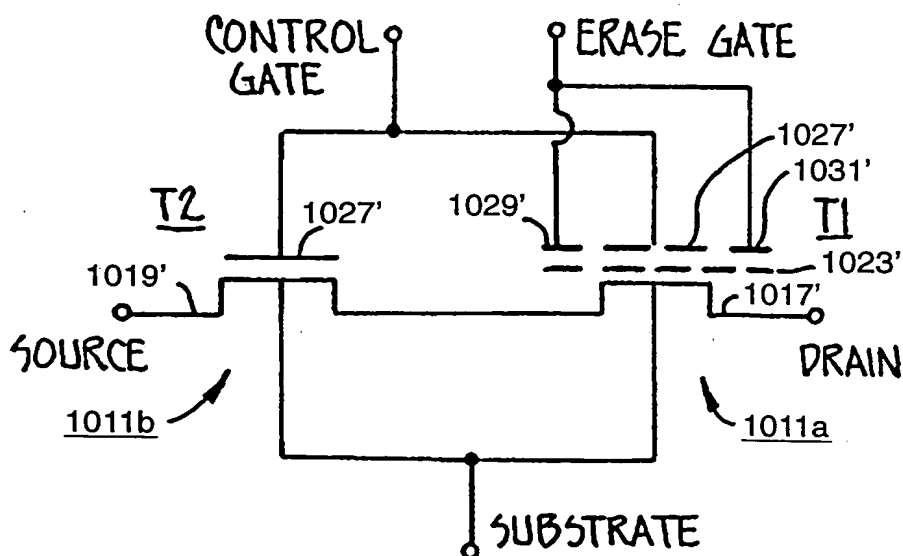


FIG. 11

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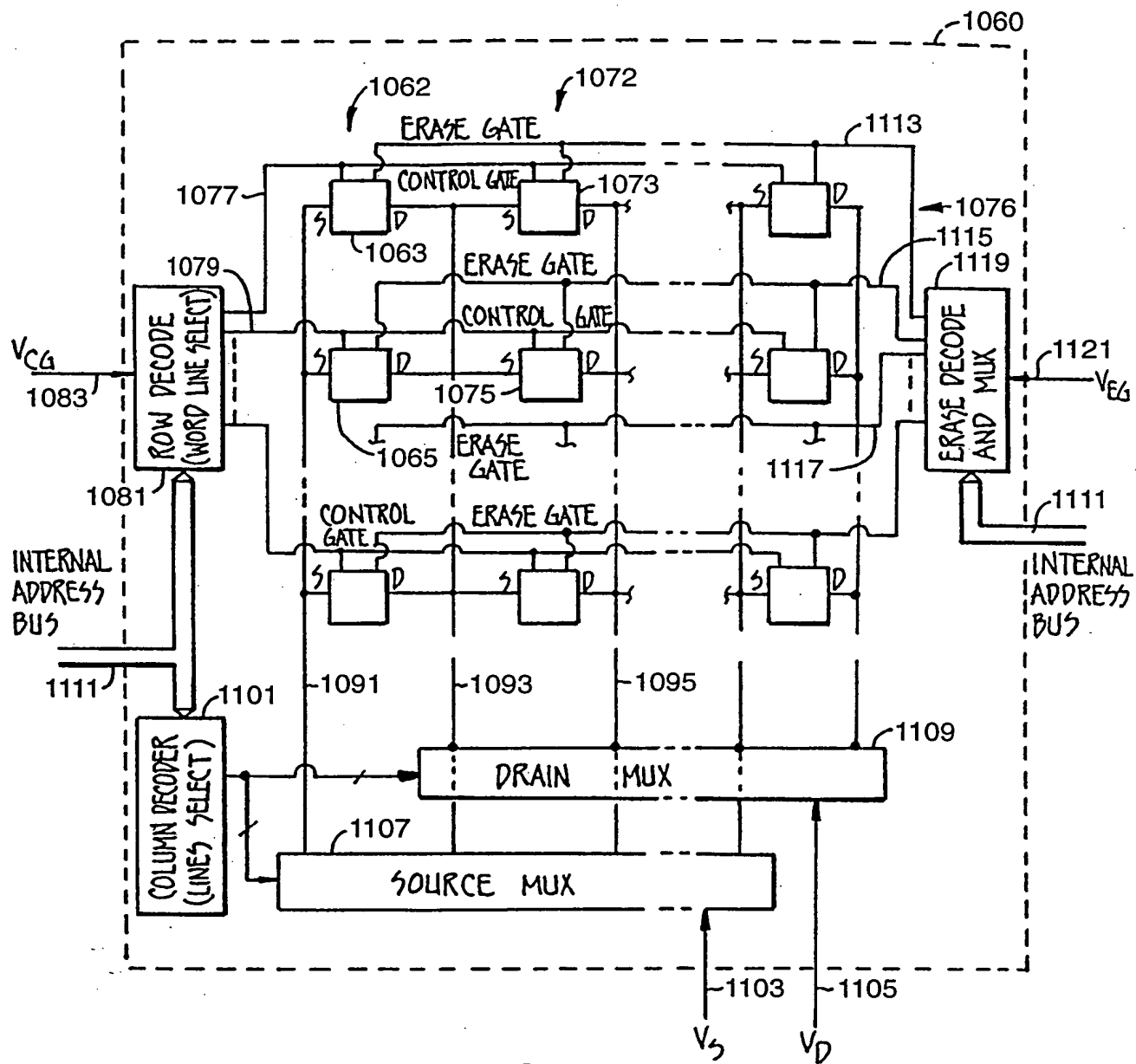


FIG. 12

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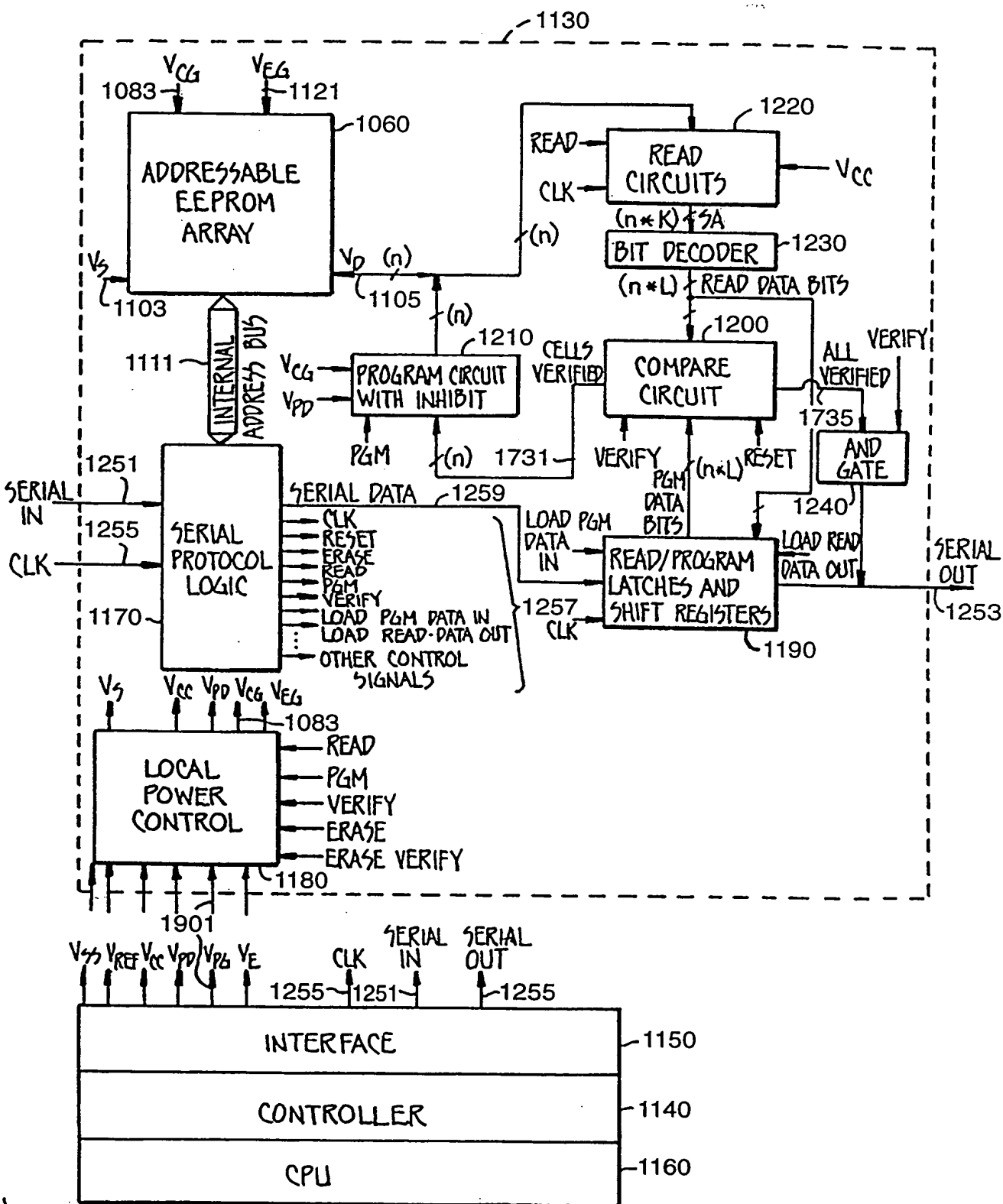


FIG. 13



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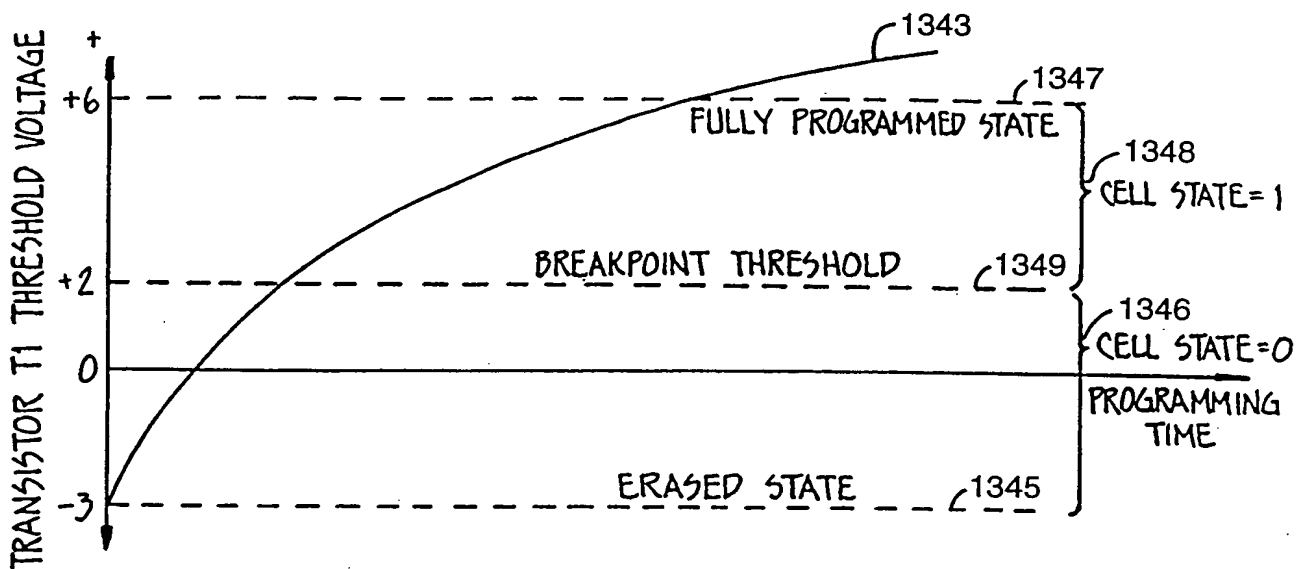


FIG. 14

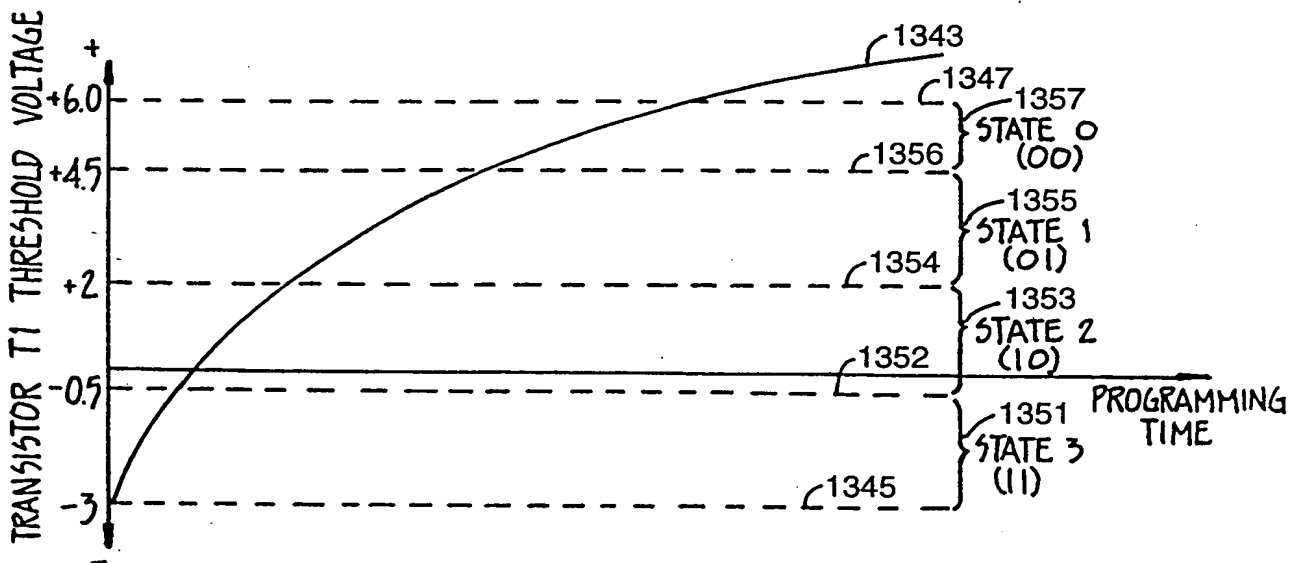


FIG. 15A

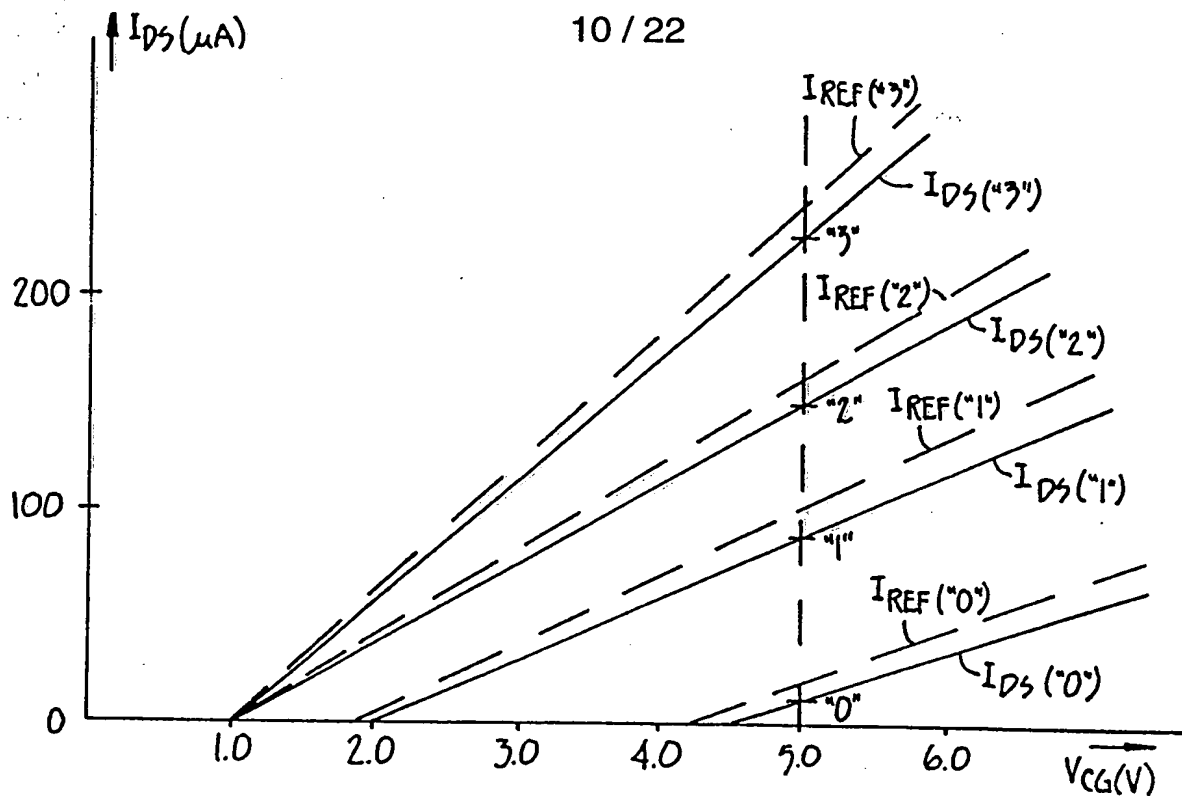


FIG._15B

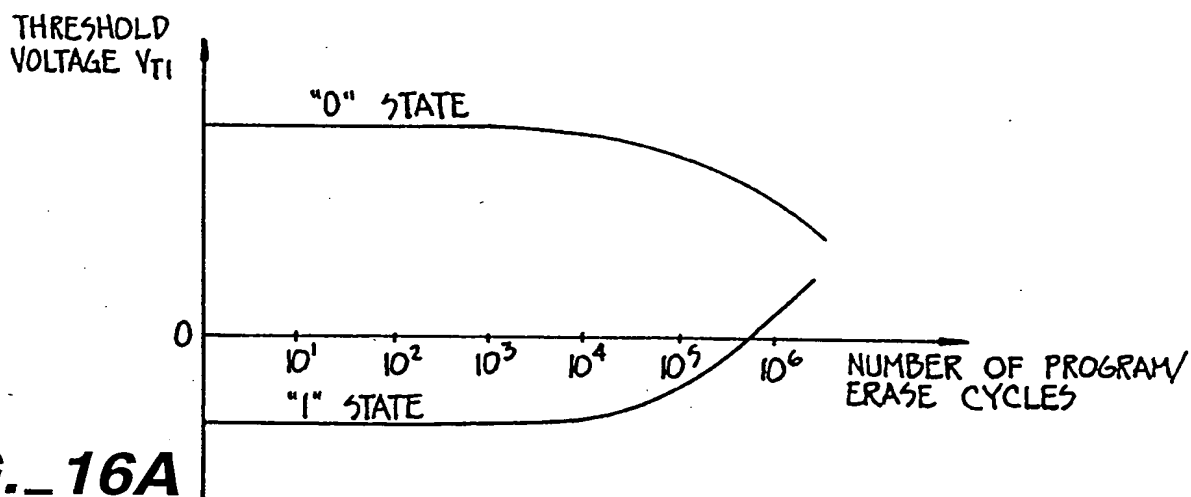


FIG._16A

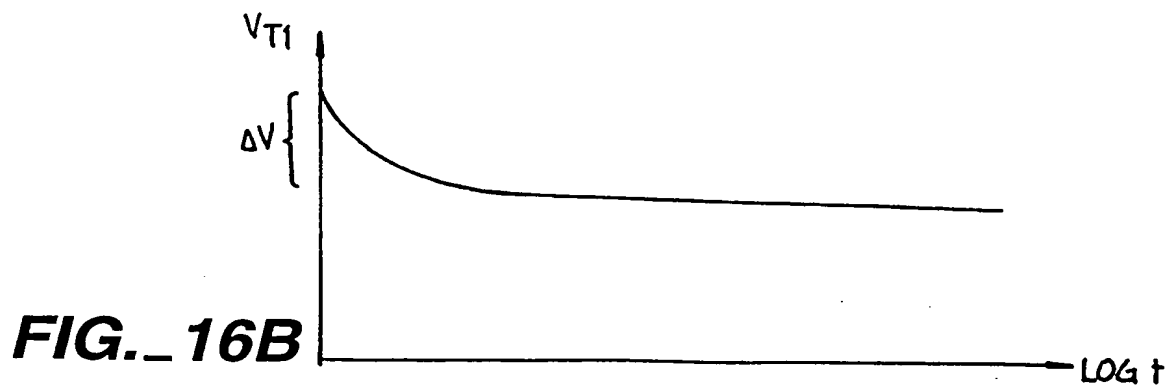


FIG._16B

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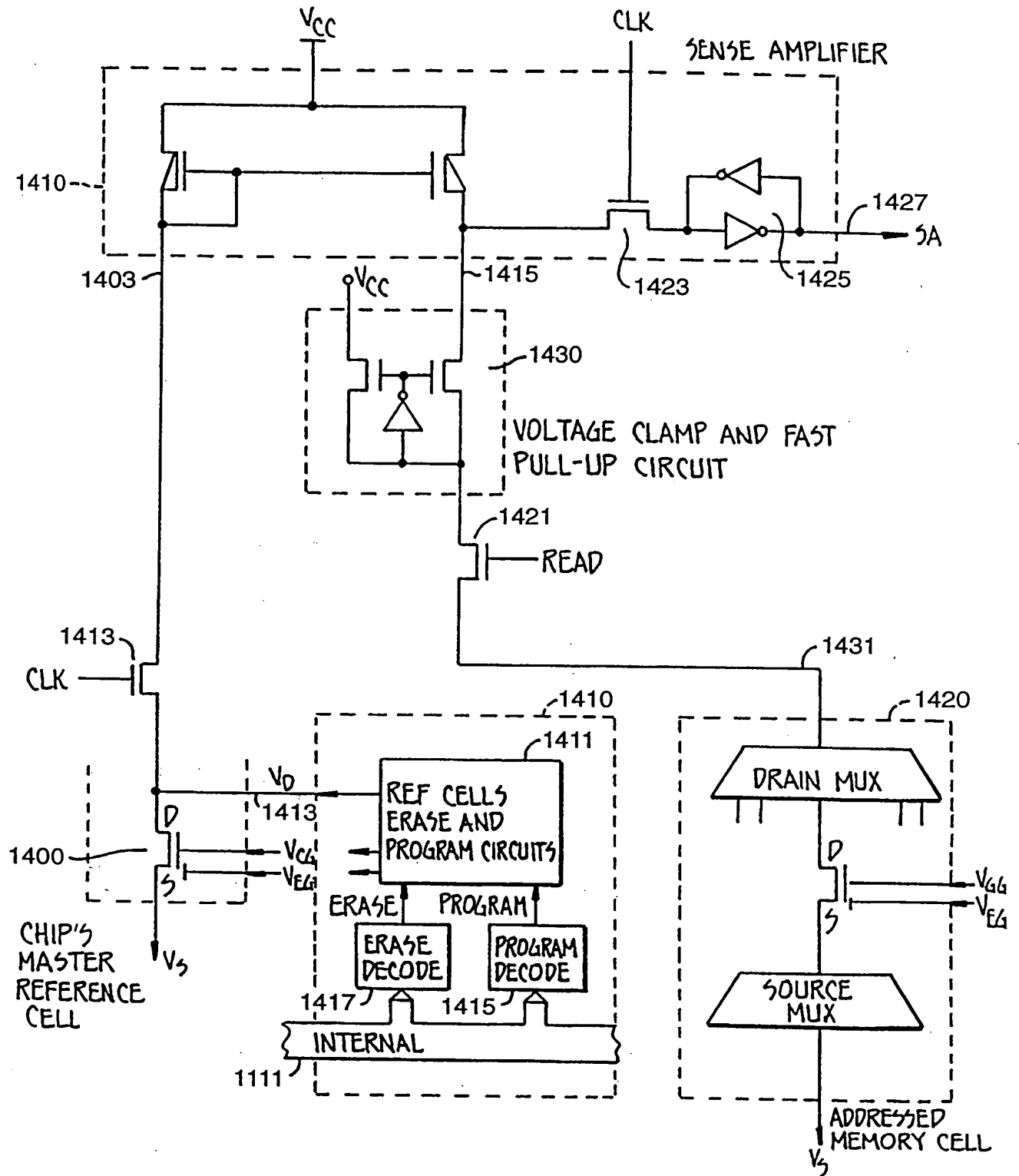
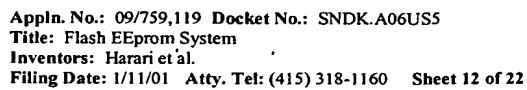


FIG. 17A



The diagram illustrates a multi-state sense amplifier circuit. At the top, a V_{CC} supply is connected to a network of transistors (1461, 1471, 1463, 1473, 1465, 1475) that form the sense amplifier. These transistors are controlled by clock signals $CLK1$, $CLK2$, and $CLK K$. The sense amplifier outputs are labeled $SA1$, $SA2$, and SAK . These outputs are connected to a $K-L$ DECODER (1480), which produces $BIT 1$, $BIT 2$, and $BIT L$ signals. The sense amplifier is also connected to a 1441 line, which is connected to a 1421 transistor (READ) that leads to the TO ADDRESSSED MEMORY CELL. The sense amplifier is also connected to a 1440 line. At the bottom, there are $MULTI-STATE$ REFERENCE CELLS (1431, 1433, 1435) connected to the 1441 line. These cells are controlled by clock signals $CLK1$, $CLK2$, and $CLK K$.

FIG. 17B

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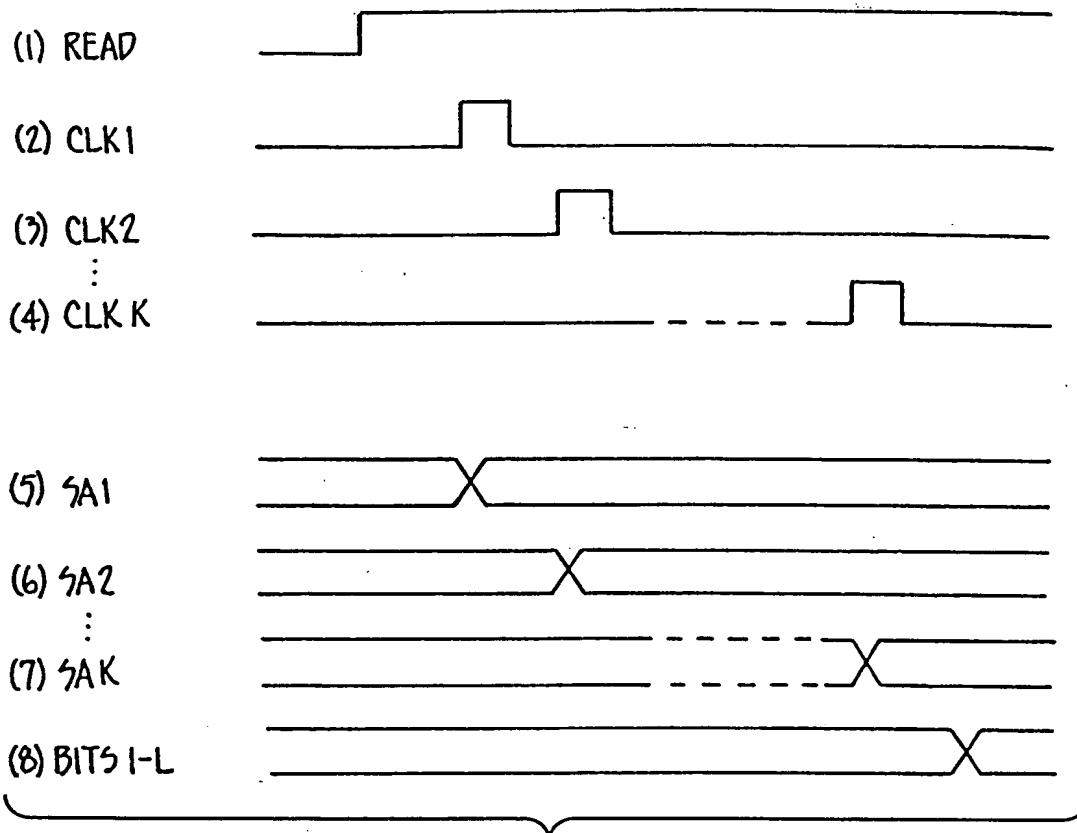


FIG. 17C

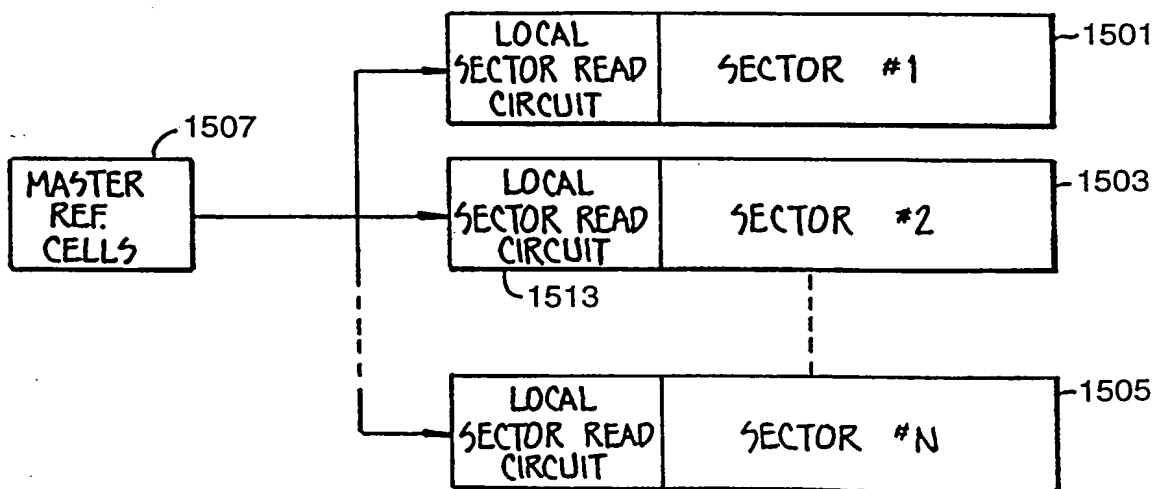


FIG. 18



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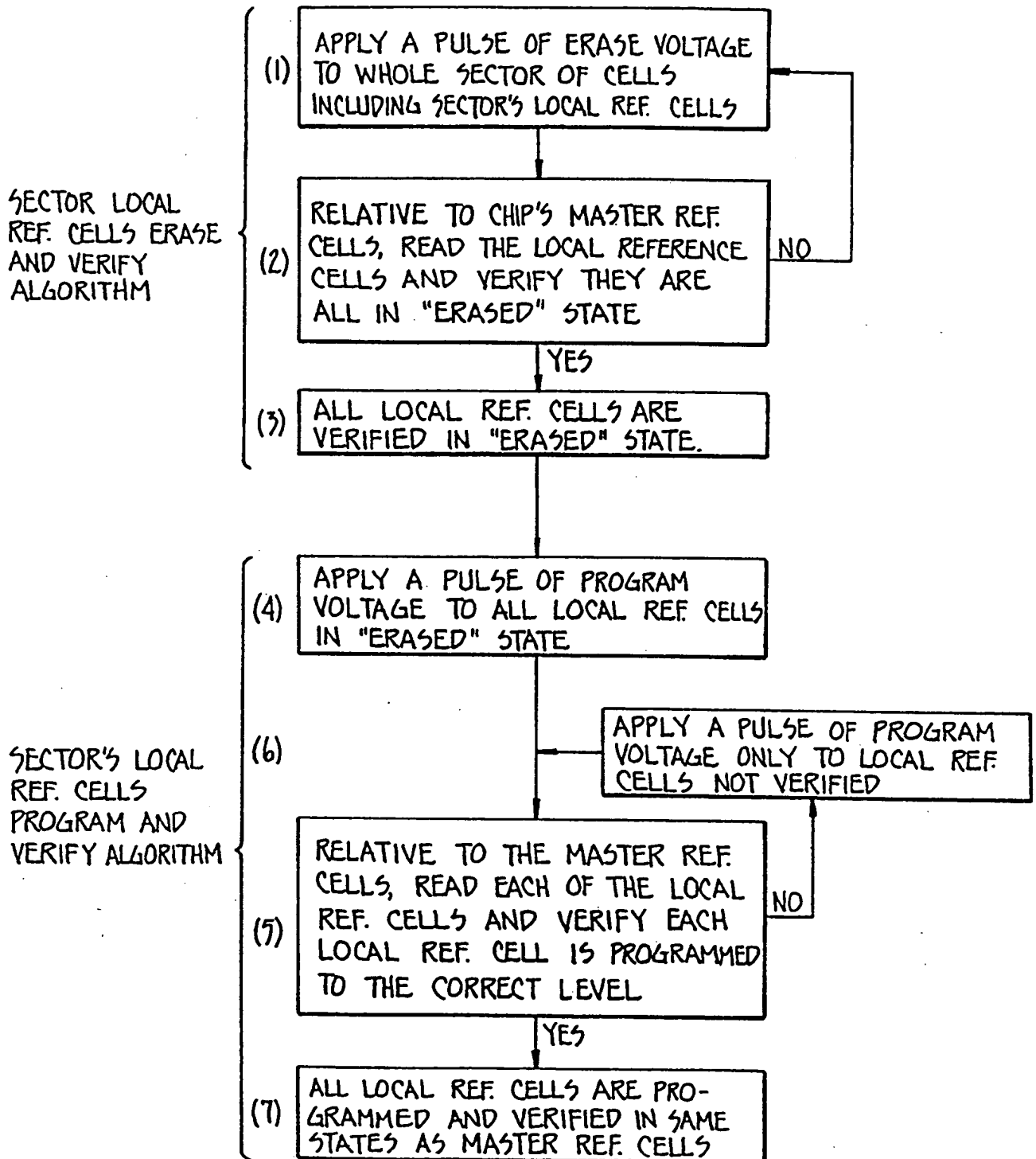


FIG. 19

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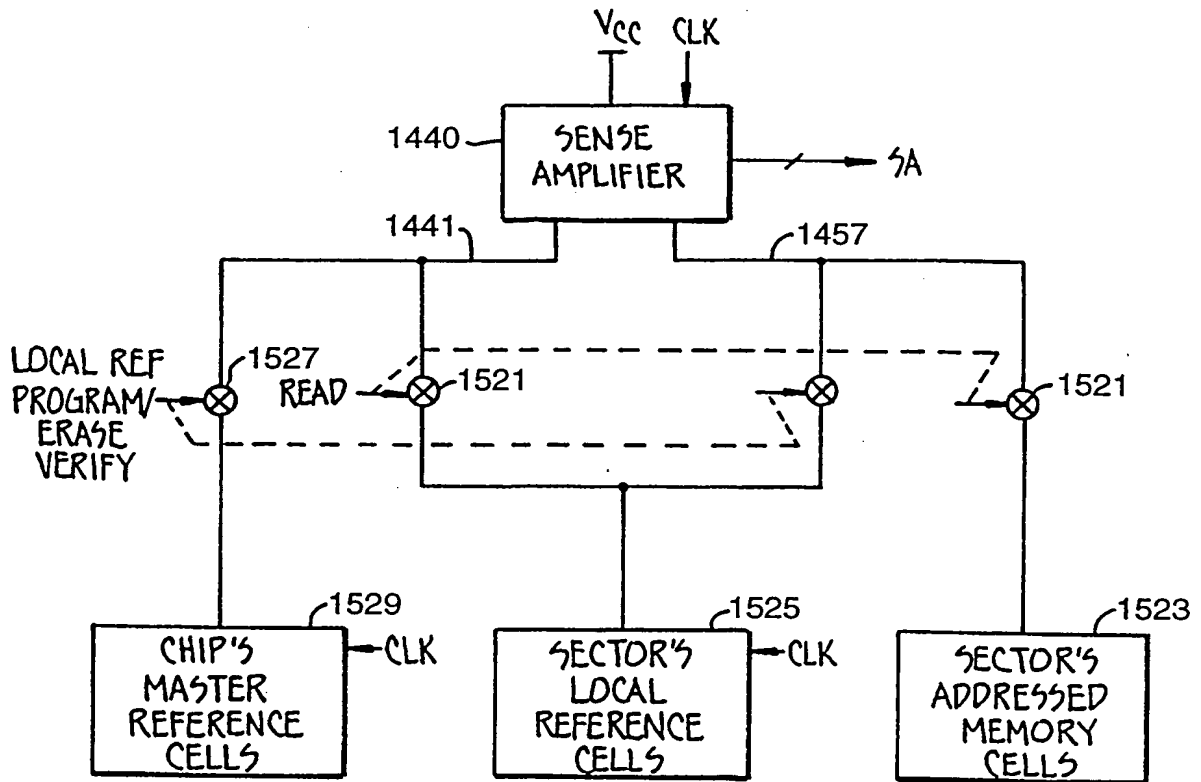


FIG. 20A

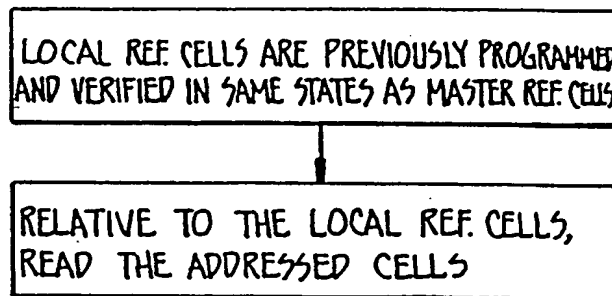
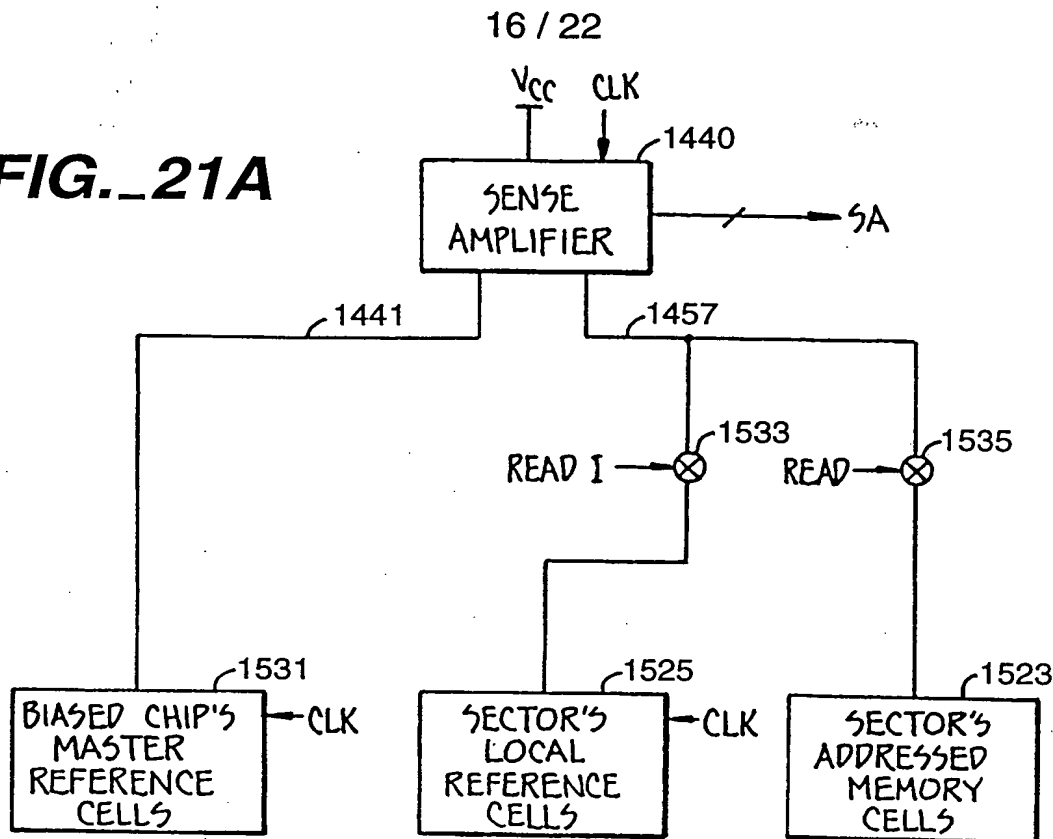


FIG. 20B

FIG. 21A



- (1) LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS
- (2) RELATIVE TO THE LOCAL REFERENCE CELLS READ THE MASTER REF. CELLS
- (3) DETERMINE THE DIFFERENCES, IF ANY AND BIAS. THE MASTER REF CELLS' CURRENTS SUCH THAT THE SAME READING IS OBTAINED RELATIVE TO THE BIASED MASTER REF. CELLS AS RELATIVE TO THE LOCAL REF. CELLS
- (4) RELATIVE TO THE BIASED MASTER REF. CELLS, READ THE ADDRESSED CELLS

FIG. 21D

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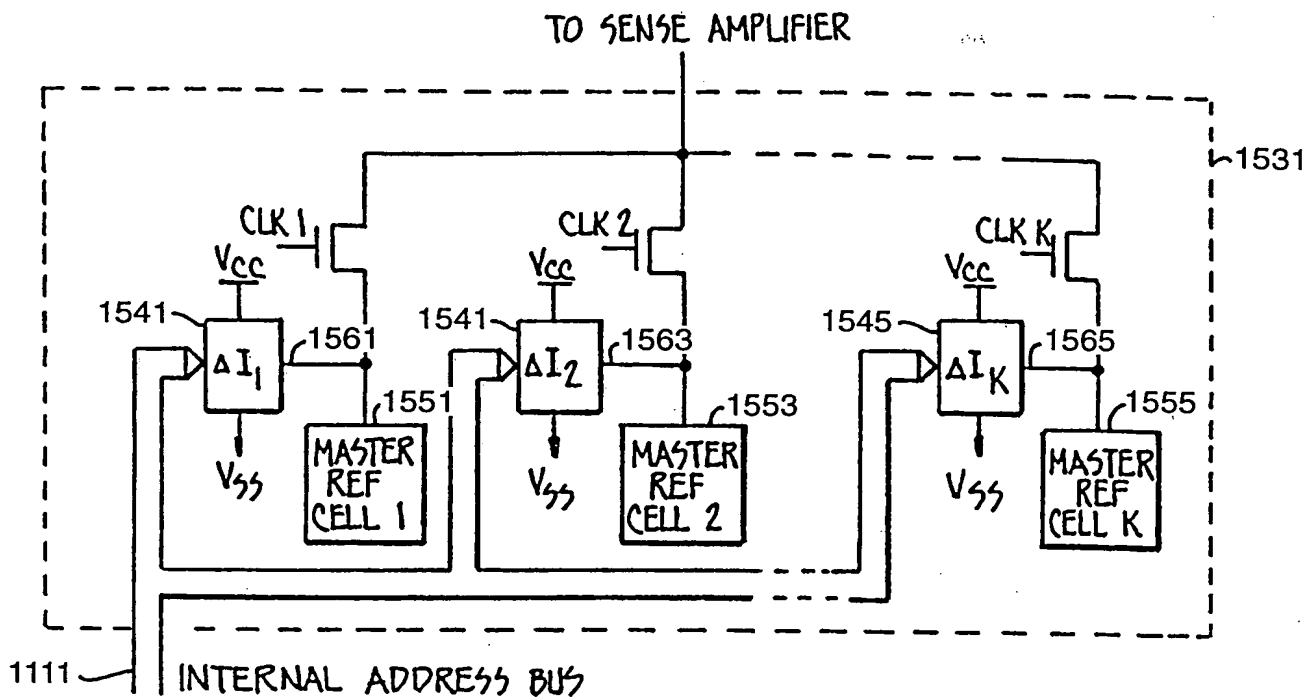


FIG. 21B

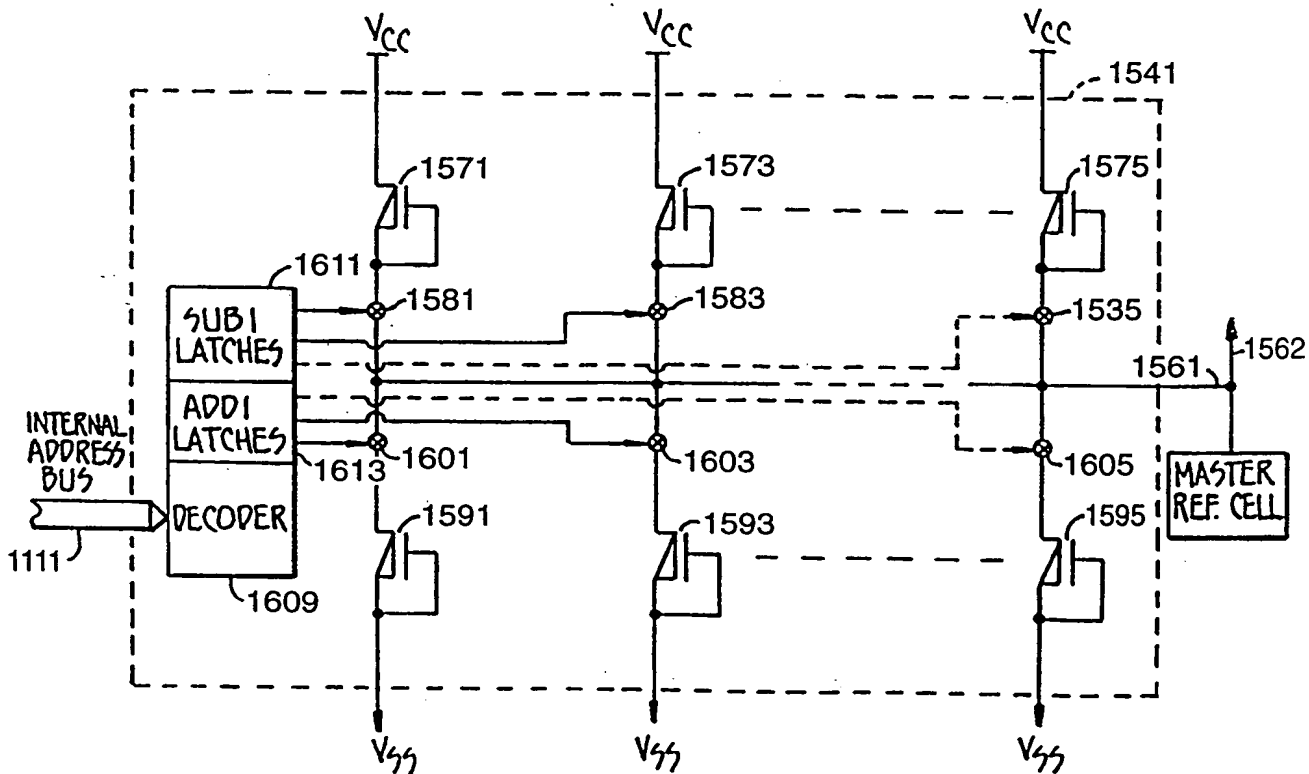
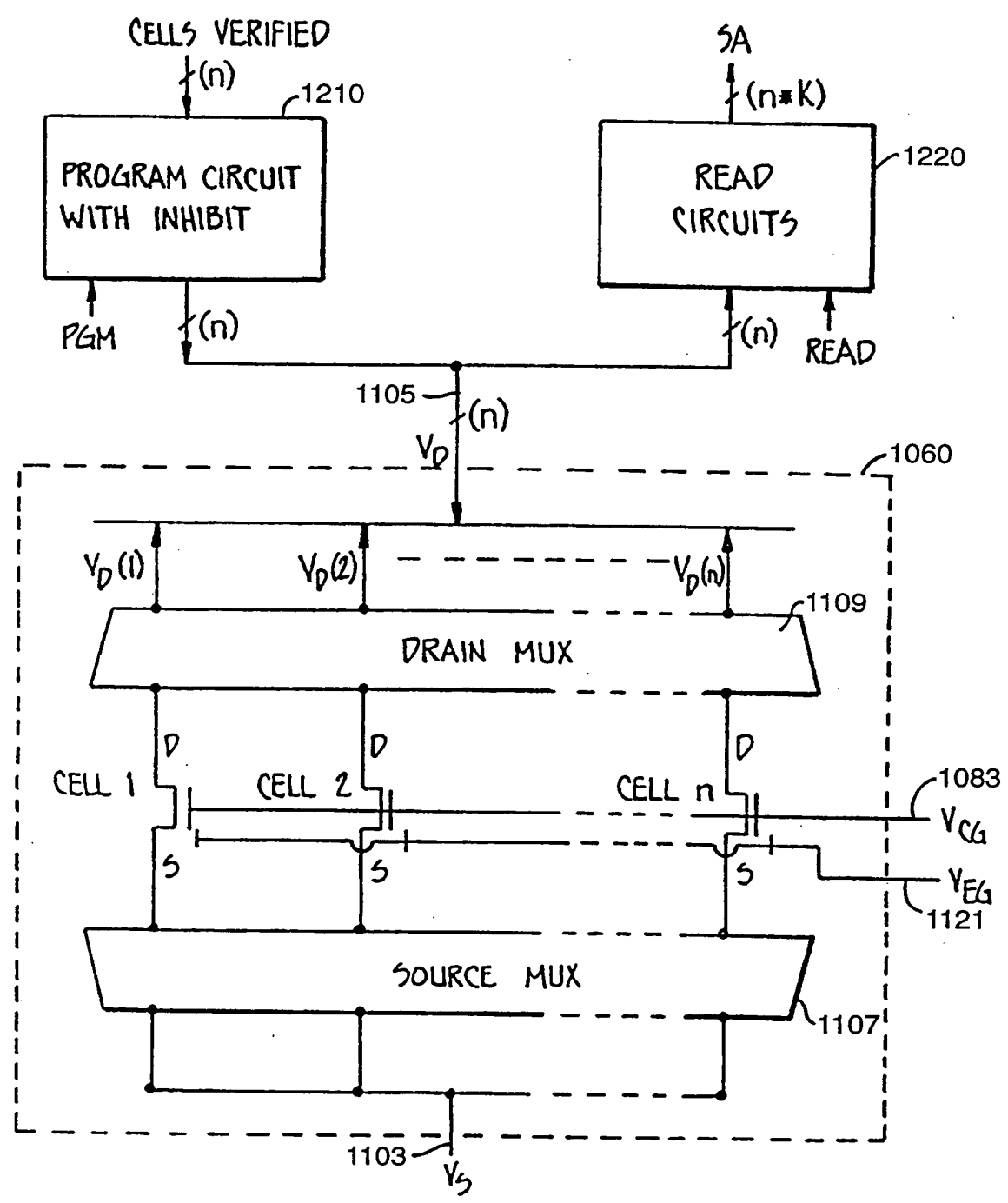


FIG. 21C

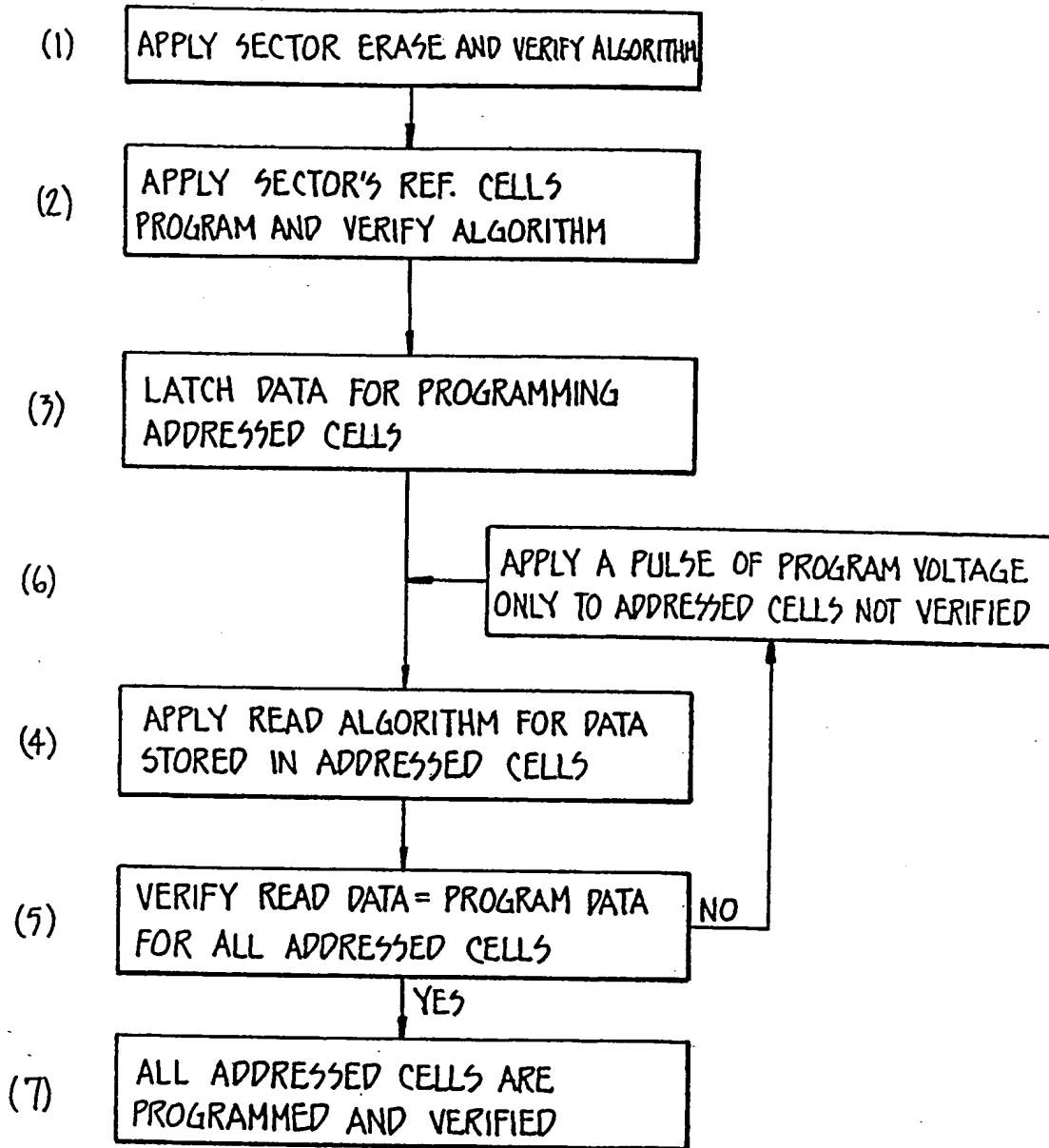


READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG. 22



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PROGRAM ALGORITHM

FIG. 23



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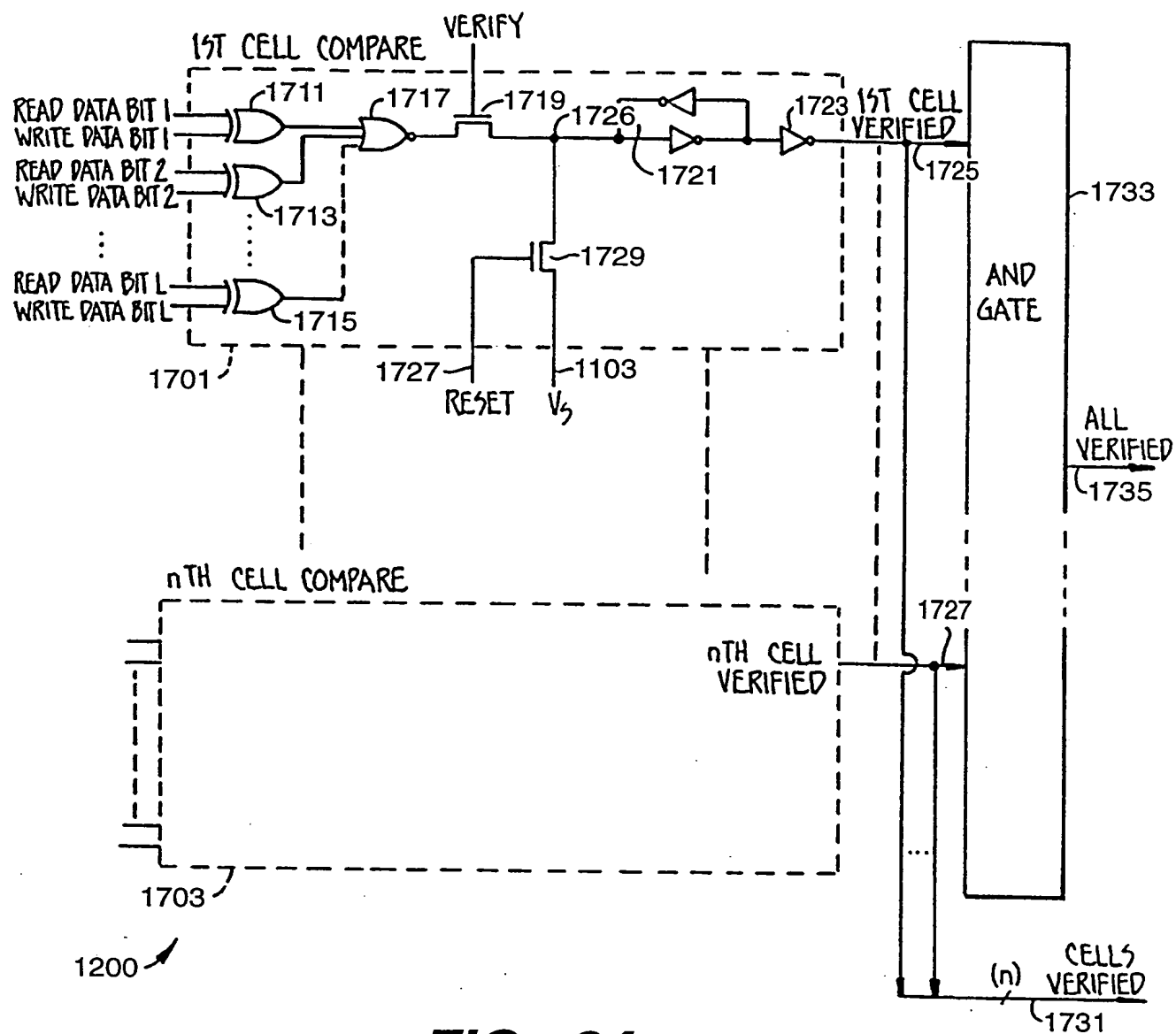


FIG. 24

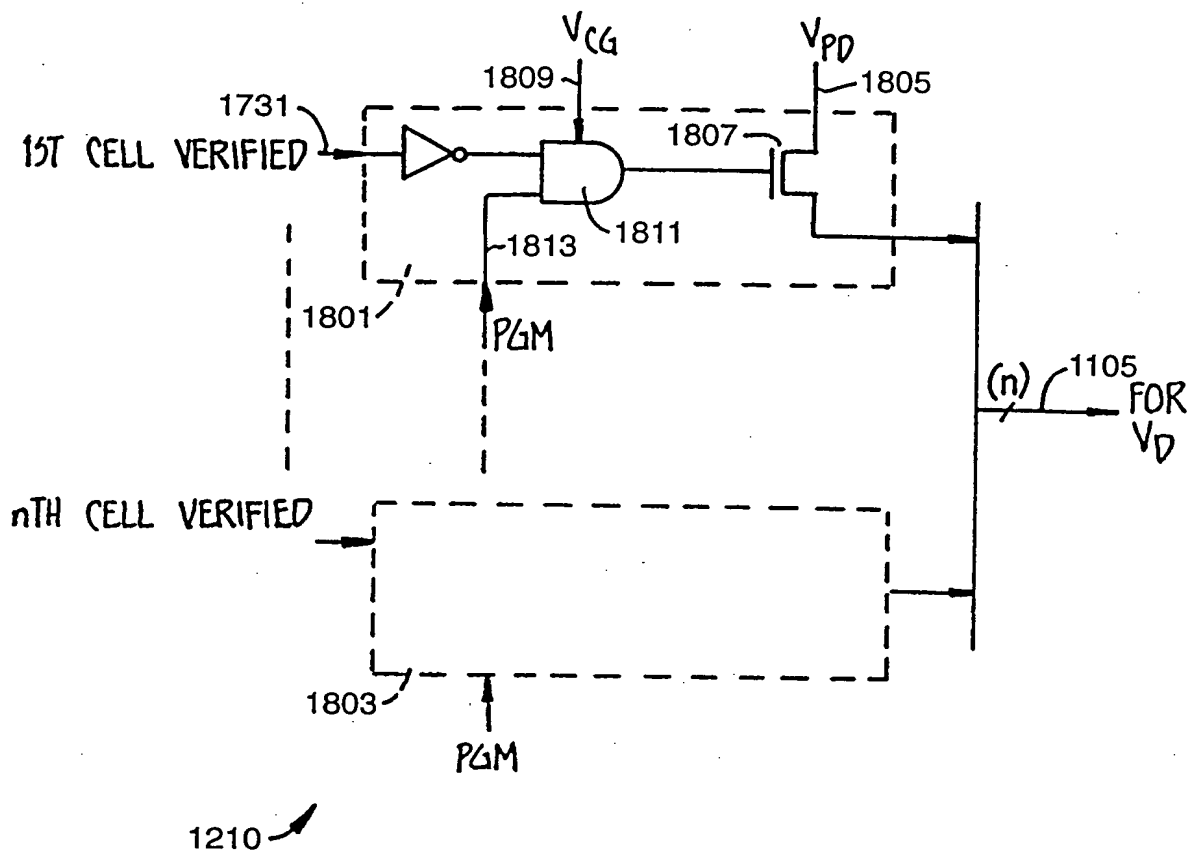


FIG. 25



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| | SELECTED CONTROL GATE V_{CG} | DRAIN V_D | SOURCE V_S | ERASE GATE V_{EG} |
|-------------------|-----------------------------------|----------------|-----------------|------------------------|
| READ | V_{PG} | V_{REF} | V_{SS} | V_E |
| PROGRAM | V_{PG} | V_{PD} | V_{SS} | V_E |
| PROGRAM VERIFY | V_{PG} | V_{REF} | V_{SS} | V_E |
| ERASE | V_{PG} | V_{REF} | V_{SS} | V_E |
| ERASE VERIFY | V_{PG} | V_{REF} | V_{SS} | V_E |

TABLE 1

FIG._26

| (TYPICAL VALUES) | READ | PROGRAM | PROGRAM VERIFY | ERASE | ERASE VERIFY |
|----------------------------|-----------|-----------|---------------------|-----------|---------------------|
| V_{PG} | V_{CC} | 12V | $V_{CC} + \delta V$ | V_{CC} | $V_{CC} - \delta V$ |
| V_{CC} | 5V | 5V | 5V | 5V | 5V |
| V_{PD} | V_{SS} | 8V | 8V | V_{SS} | V_{SS} |
| V_E | V_{SS} | V_{SS} | V_{SS} | 20V | V_{SS} |
| UNSELECTED CONTROL GATE | V_{SS} | V_{SS} | V_{SS} | V_{SS} | V_{SS} |
| UNSELECTED BIT LINE | V_{REF} | V_{REF} | V_{REF} | V_{REF} | V_{REF} |

$V_{SS} = 0V$, $V_{REF} = 1.5V$, $\delta V = 0.5V - 1V$

TABLE 2

FIG._27

+